

Model : P75/55IMx

Intel Merom CPU + PM965 + ICH8-M Chipset
Santa Rosa plantfrom (No supported AMT)

Revision History		
	08/2006	Initial Rev.RA
	09/2006	Rev.A1
	11/2006	Rev.A2
	01/2007	Rev.B
	03/2007	Rev.C

PCB P/N: 37GP55000-C0
PCBA P/N: 82GP55000-C0

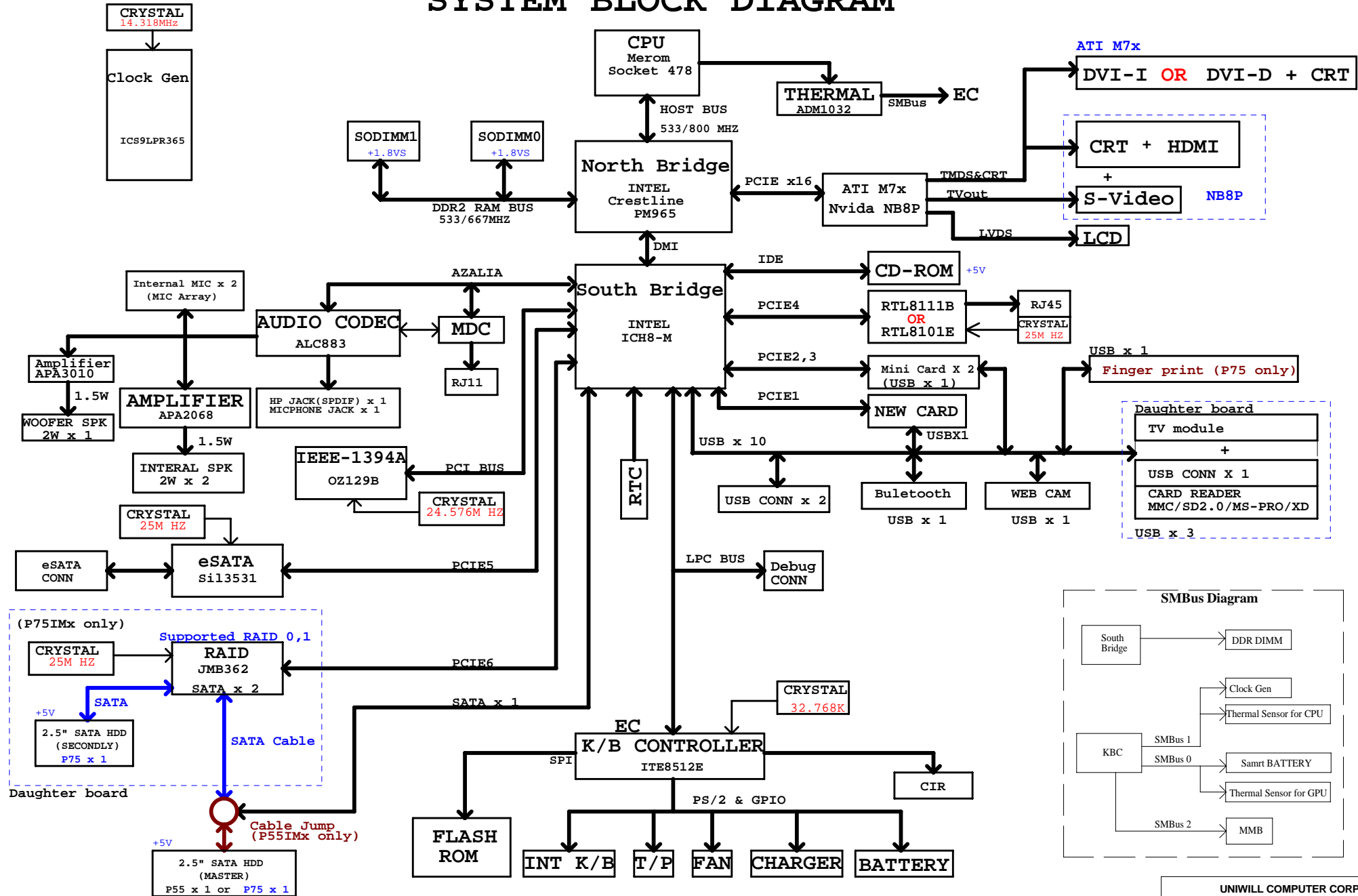
PG01 INDEX
PG02 SYSTEM BLOCK DIAGRAM
PG03 POWER DIAGRAM & SEQUENCE
PG04 GPIO & POWER CONSUMPTION
PG05 CPU Merom-1/2
PG06 CPU Merom-2/2
PG07 CLOCK GEN SLG8SP510
PG08 NB HOST -1/5
PG09 NB VGA_PCIEXPR-2/5
PG10 NB DDR_MEM SYSTEM-3/5
PG11 NB POWER-4/5
PG12 NB VSS_NCTF-5/5
PG13 DDR2 SODIMM
PG14 DC IN / Termination / SMP
PG15 PWR S/W& LED CONN /INVERTER
PG16 SB ICH8-MDH -1/3
PG17 SB ICH8-MDH -2/3
PG18 SB ICH8-MDH -3/3
PG19 HDD / CD-ROM CONN

PG20 minCARD/New Card/FigerPrint
PG21 USB/ IO/BT/ FP/WCAM CONN
PG22 AUD PWR / FAN CTL/ HSCR Cap
PG23 GIGA LAN RTL8111B
PG24 IEEE1394A OZ129
PG25 EC IT8512 / BIOS / TP CON
PG26 VGA CONN
PG27 CPU_CORE (MAX8771)
PG28 1.5VS/1.8VS MAX8716 /LDO
PG29 +3.3V/+5V MAX8774
PG30 VCC SW / VIN SW
PG31 BATT IN / Charger
PG32 e-SATA (Sil3531)
PG33 CODEC (ALC883) & AMP(APA2068)
PG34 PHONE JACK & CONN & MDC
PG35 Appendix A. Ver.AtoA1 History
PG36 Appendix B. Ver.AltoA2 History
PG37 Appendix C. Ver.RBltoRC History

UNIWILL COMPUTER CORP.			
File		P75/55IMx	
Size	Document Number	INDEX	
	3581	Rev C	
Date	Tuesday, March 13, 2007	Sheet	1 of 37

P75/55IMx

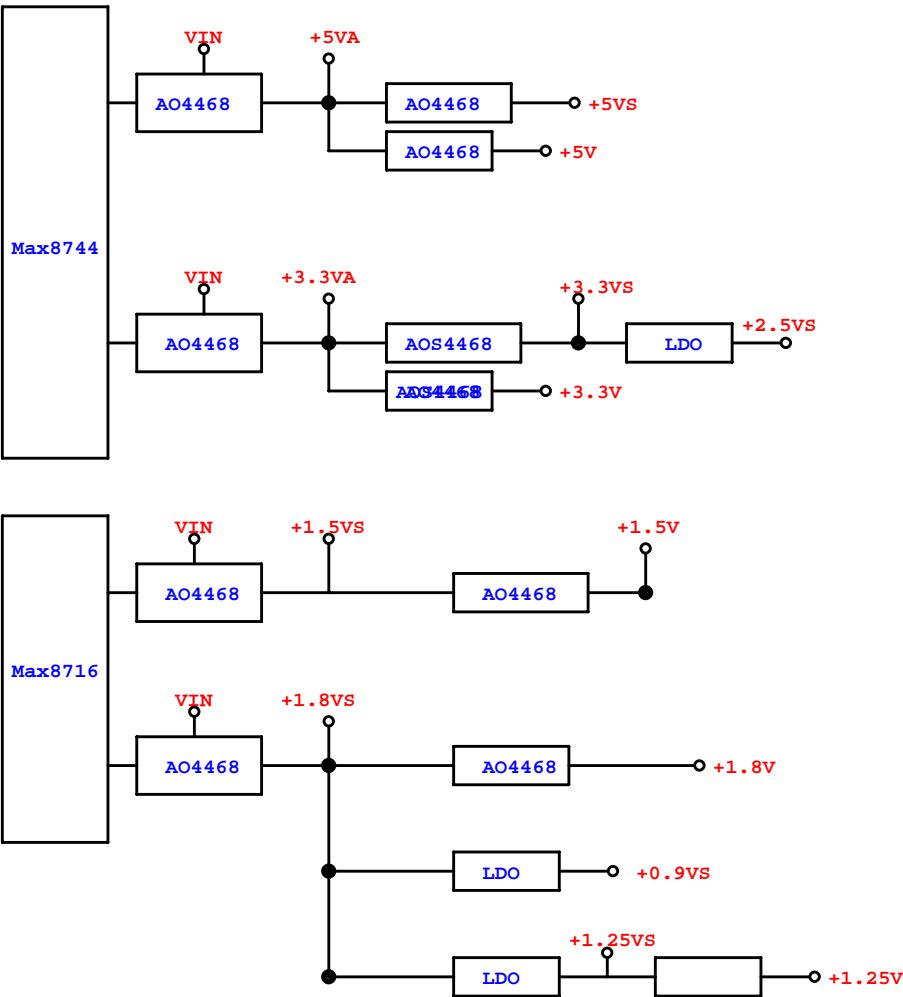
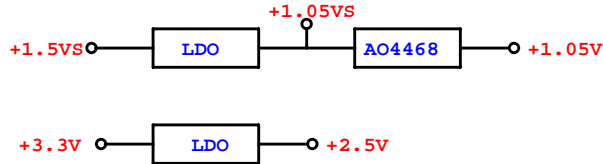
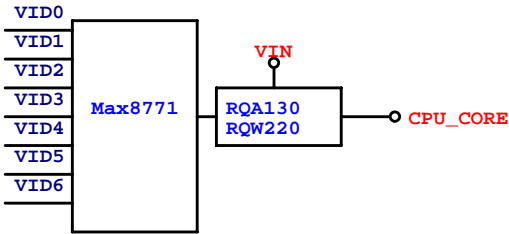
SYSTEM BLOCK DIAGRAM



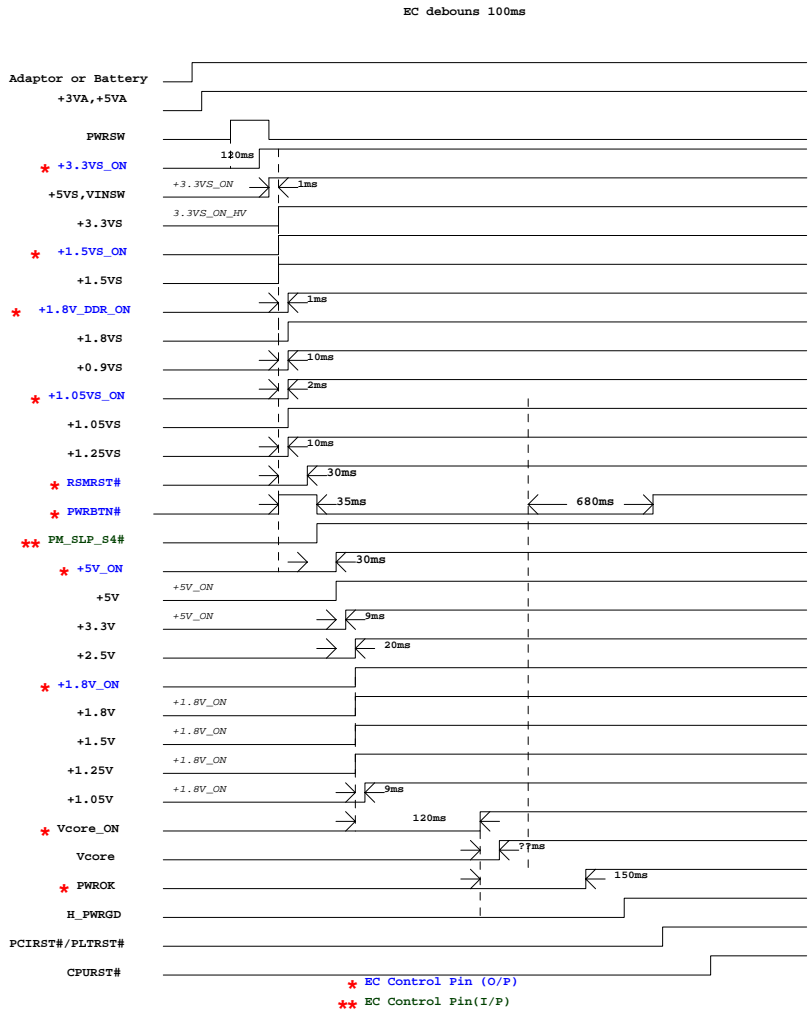
UNIWILL COMPUTER CORP.

P75/55IMx			
Size	Document Number	Rev	C
3561	SYSTEM BLOCK DIAGRAM		
Date	Tuesday, March 13, 2007	Sheet	2 of 37

POWER BLOCK DIAGRAM



Poewr On Sequence



ICH8-M GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQ#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	N.C (TACH3)
GPIO8	N.C
GPIO9	N.C (WOL_EN)
GPIO10	N.C (ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	N.C (GLAN_DOCK#)
GPIO14	N.C (NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	N.C (TACH0)
GPIO18	N.C
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	N.C (SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	N.C (HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8512E GPIO	
GPA0	PM_RSMRST#
GPA1	SUSPEND_LED
GPA2	SILENT_LED
GPA3	RF_LED
GPA4	CAPS_LED
GPA5	NUM_LED
GPA6	SCROLL/3G_LED
GPA7	EXTTS#0
GPB0	PM_SLP_S4#
GPB1	PM_SLP_S3#
GPB2	CMI_TX
GPB3	SMB_CLK0
GPB4	SMB_DAT0
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	QRT_STATE
GPC0	CMI_RX
GPC1	SMB_CLK1
GPC2	SMB_DAT1
GPC3	KEY_OUT16
GPC4	RF_SW#
GPC5	KEY_OUT17
GPC6	BTL_BEEP
GPC7	SILENT#
GPD0	EC_PREST#
GPD1	PWRBTN#
GPD2	MUTE
GPD3	EC_EXTSMI#
GPD4	N.C
GPD5	SMP1_EN#
GPD6	CHG_ON
GPD7	LCDSW
GPE0	PWRSW
GPE1	SET_V
GPE2	PWROK
GPE3	BT_ON
GPE4	LID#
GPE5	CPPE#
GPE6	FAN_SPD#
GPE7	PCI_RST#
GPF0	EC_CPU_200MHz
GPF1	N.C
GPF2	CHG_G_LED
GPF3	CHG_R_LED
GPF4	TP_CLK
GPF5	TP_DATA
GPF6	N.C
GPF7	N.C
GPG0	SB_RTCRST
GPG1	EC_WDOG OK
GPG2	FLFRAME#
GPG6	MPWORK
GPH0	+1.8V_ON
GPH1	+1.8V_DDR_ON
GPH2	VCORE_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	+1.05VS_ON
GPH6	+1.5VS_ON

ITE8512E GPIO	
GPI0	BATT_TEMP
GPI1	ADAPTOR_I
GPI2	ADAP_IN
GPI3	BAT_CHG_I
GPI4	BAT_I
GPI5	CPU_PWR
GPI6	DDR2_TEMP
GPI7	VGA_TEMP
GPJ0	EC_BRGHT
GPJ1	CHG_I
GPJ2	FAN_CTRL0
GPJ3	BROWSER#
GPJ4	MAIL#
GPJ5	PM_THROTTLING#

Merom CPU				
	CPU	CORE(V)	ICC(A)	W
IMVP-6+		1.25	44.0	46.2

Crestline			
VCC	ICC(mA)	W	TEMP(°C)
+3.3V	320	1.056	105
+1.8VS	2860	5.148	
+1.5V	76	0.114	
+1.25V	1100	1.375	
+1.05	4140	4.347	

ICH8-M			
VCC	ICC(mA)	mW	TEMP(°C)
+5V	2	10	70
+5VS	1	5	
+3.3V	556	1834.8	
+3.3VS	159	524.7	
+1.5V	2400	3600	
+1.25V	50	62.5	
+1.05V	1131	1187.55	

ITE8512E			
VCC	ICC(mA)	mW	TEMP(°C)
+3.3V	100	330	70

CLOCK GENERATOR			
VCC	ICC(mA)	mW	TEMP(°C)
+3.3V	270	891	70

AD1986A			
VCC	ICC(mA)	mW	TEMP(°C)
+3.3V(DVDD)	52	171.6	70
+5V(AVDD)	73	365	

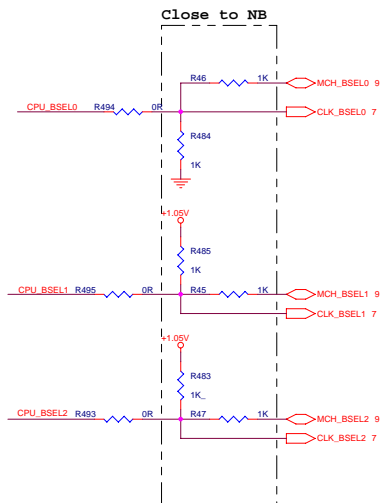
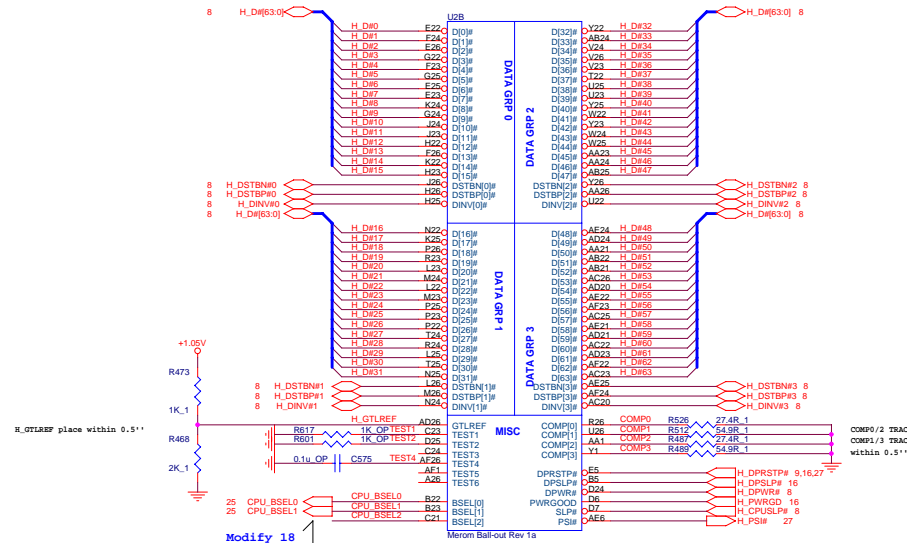
APA2068			
VCC	ICC(mA)	mW	TEMP(°C)
+5V	20	100	85

ADM1032			
VCC	ICC	mW	TEMP(°C)
+3.3V	170uA	0.56	150

OZ129B			
VCC	ICC(mA)	mW	TEMP(°C)
+3.3V	50	165	70
+1.8V	50	90	

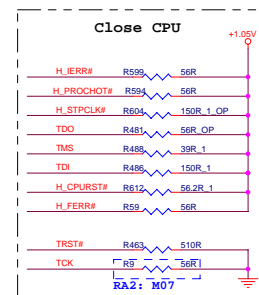
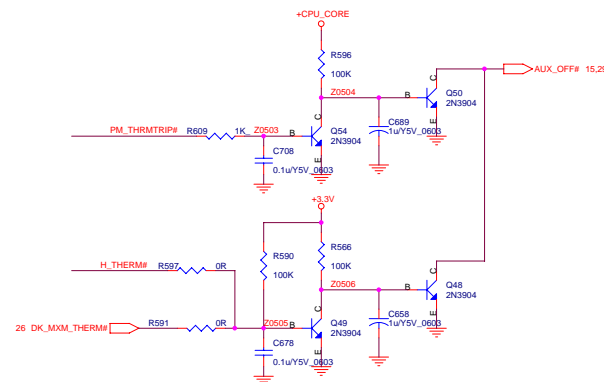
RTL8111B			
VCC	ICC(mA)	mW	TEMP(°C)
+3.3VS	103	339.9	70
+1.8VS	198	356.4	
+1.5VS	367	550.5	

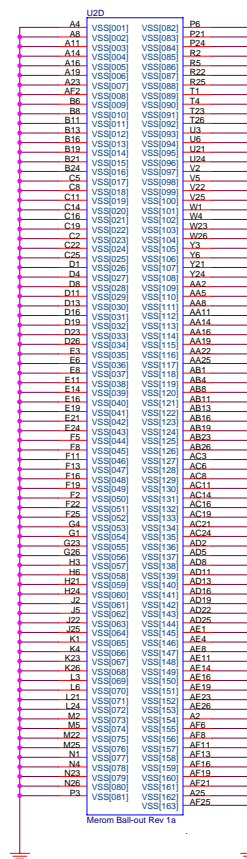
Si13531			
VCC	ICC(mA)	mW	TEMP(°C)
+3.3V	TBD		70
+1.8V	TBD		

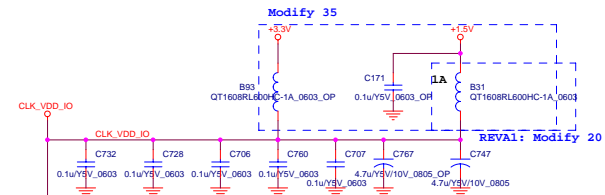
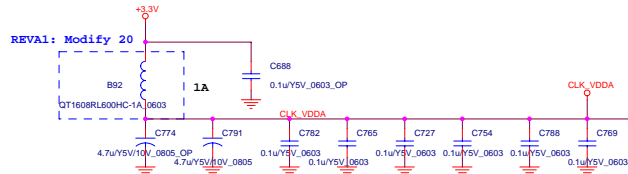
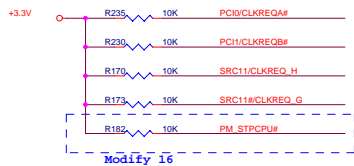


If used, pull-up change from
56R to 68R(Intel recommend).

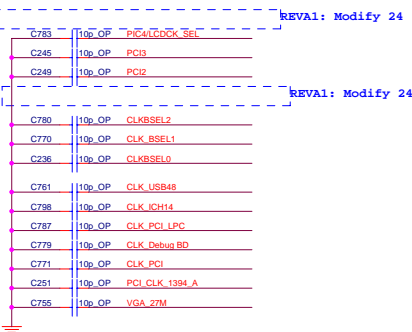
Intel recommend 512K 18'



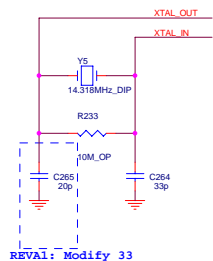




Reserved FOR EMI



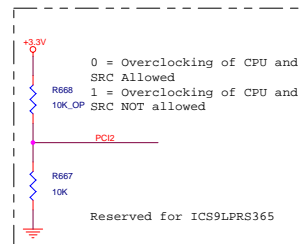
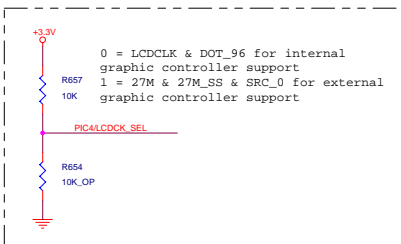
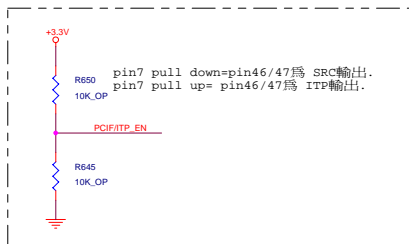
	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ
PSB800	0	1	0	200		
PSB667	0	1	1	166	33	100
PSB533	0	0	1	133		

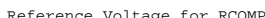


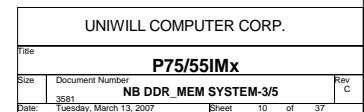
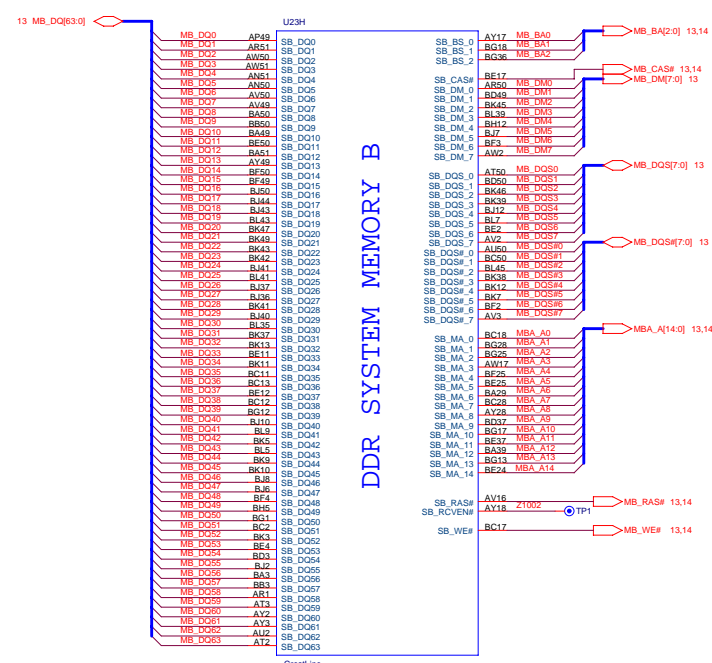
$$C_e = 2 * C_L - (C_s + C_1)$$

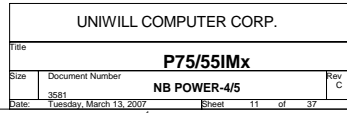
CL = Crystal Load Cap = 20P
C1 = IC internal Cap = 5p
Ce = 2p
Ce = Crystal external Cap = 33P

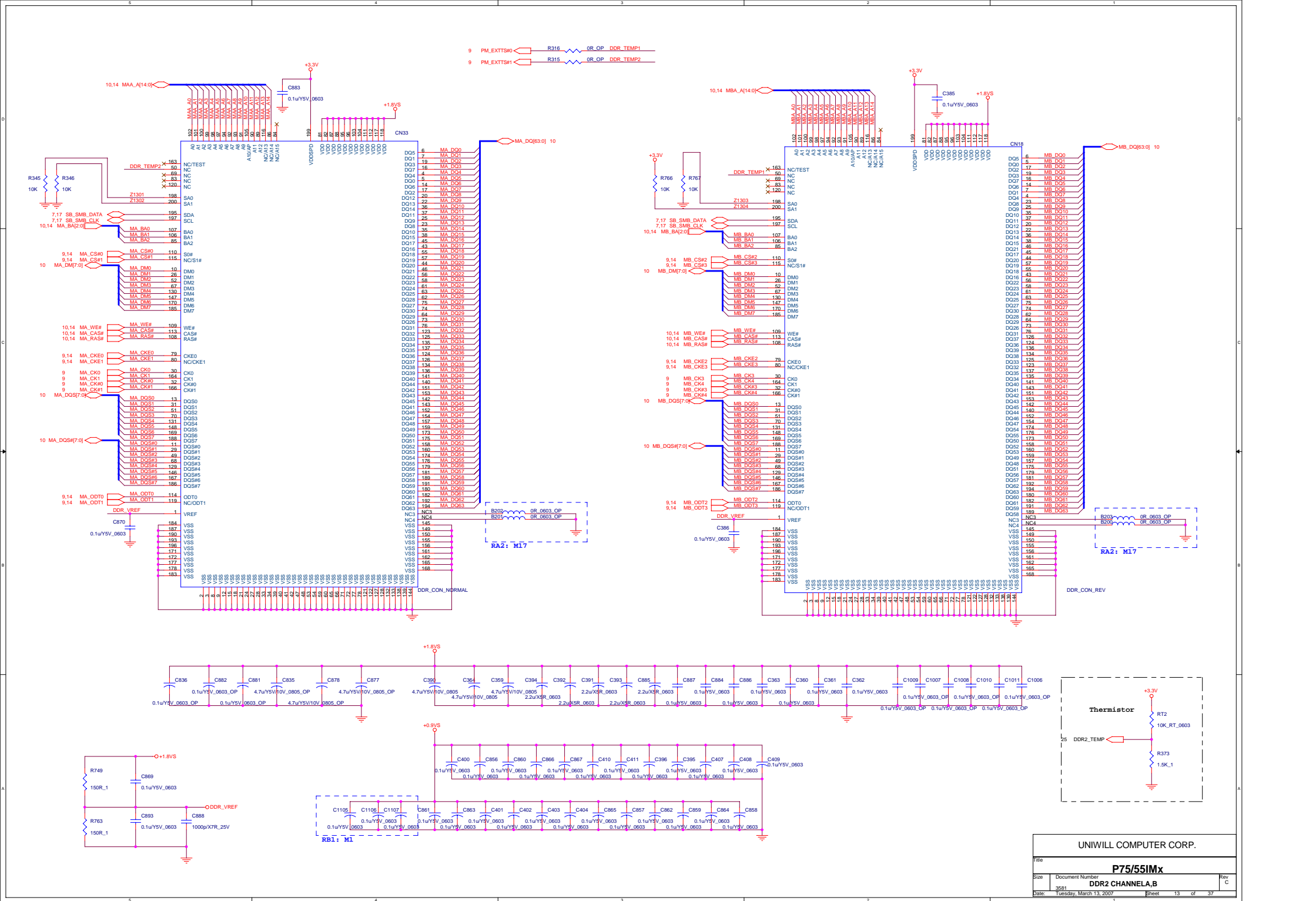
CLK REQ	From	O/P
A	ICH_SATA	SRC2
B	MCH_GCLK	SRC4
H	GLAN	SRC10
G	MINICARD1	SRC9

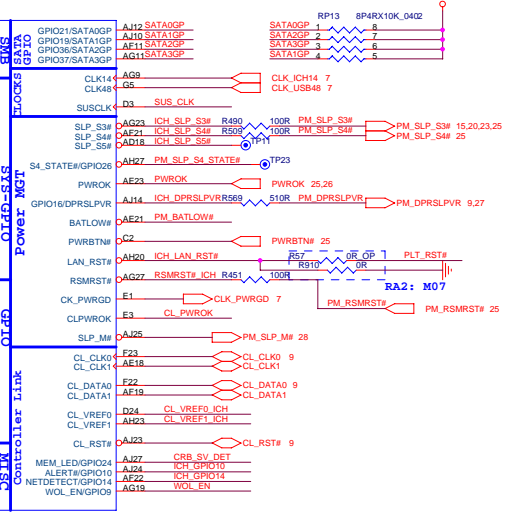
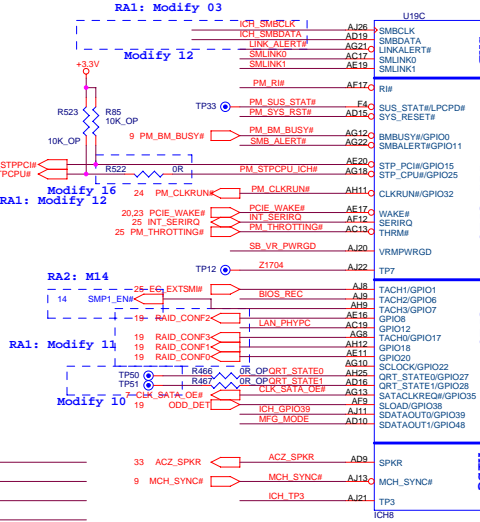
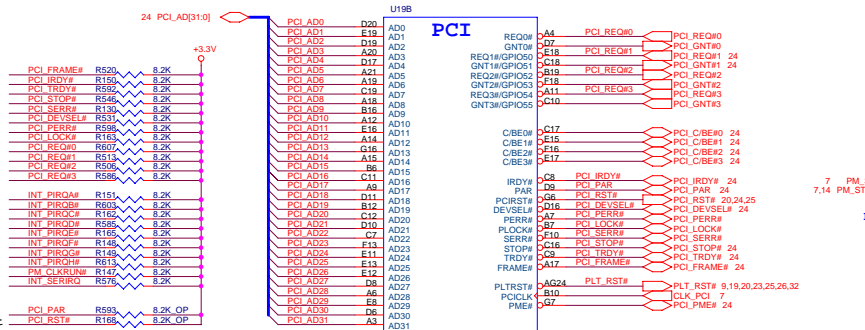




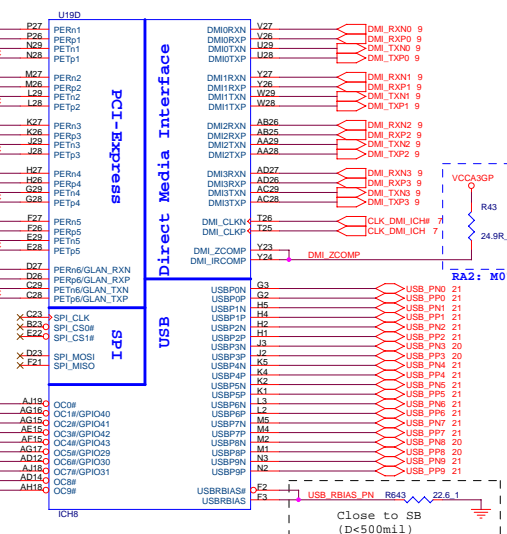
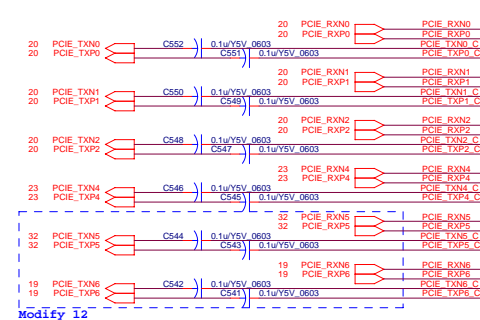
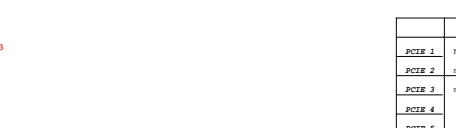
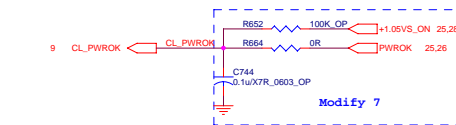
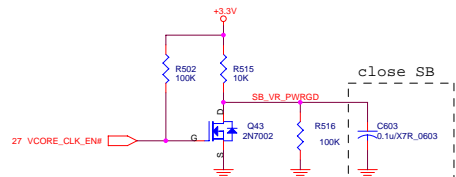
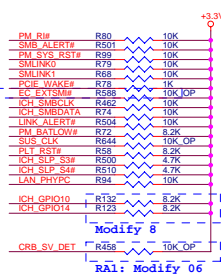
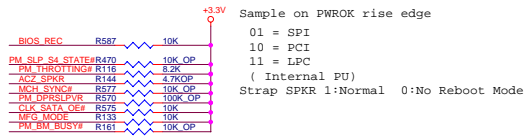






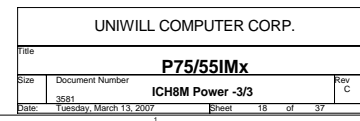


Resume Power GPIO [8:10] [12:15] [25:28]

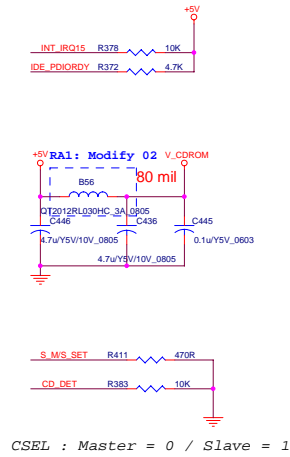
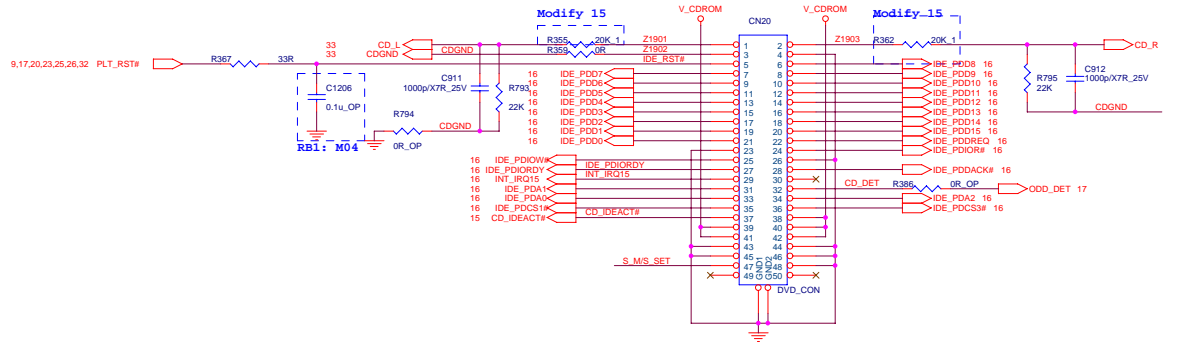


	P55	P75
USB0	CH1(USB)	CH1(USB)
USB1	CH5(USB)	CH5(USB)
USB2	WEB_CAM	WEB_CAM
USB3	MINI_CARD1	MINI_CARD1
USB4	CH4(USB)	CH4(USB)
USB5	NIMICARD2	NIMICARD2
USB6	BLUETOOTH	BLUETOOTH
USB7	CardReader	X (PS1394)
USB8	NEW_CARD	NEW_CARD
USB9	3G / TV	3G / TV

UNIWILL COMPUTER CORP.

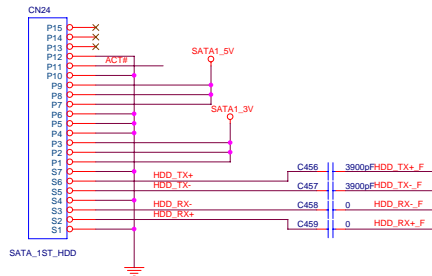


CR-ROM

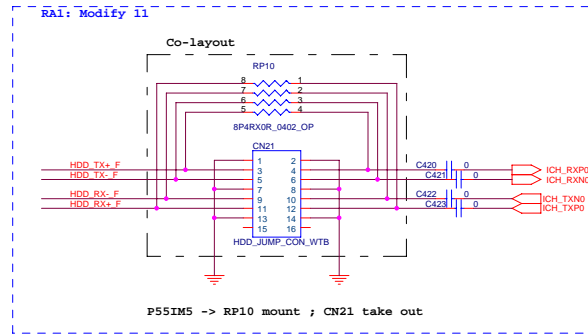


CSEL : Master = 0 / Slave = 1

MASTER HDD

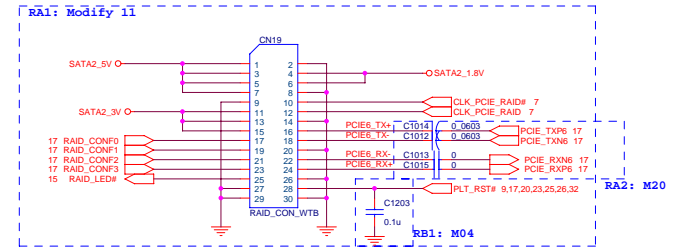


Cable Jump CONN



P55IM5 -> RP10 mount ; CN21 take out

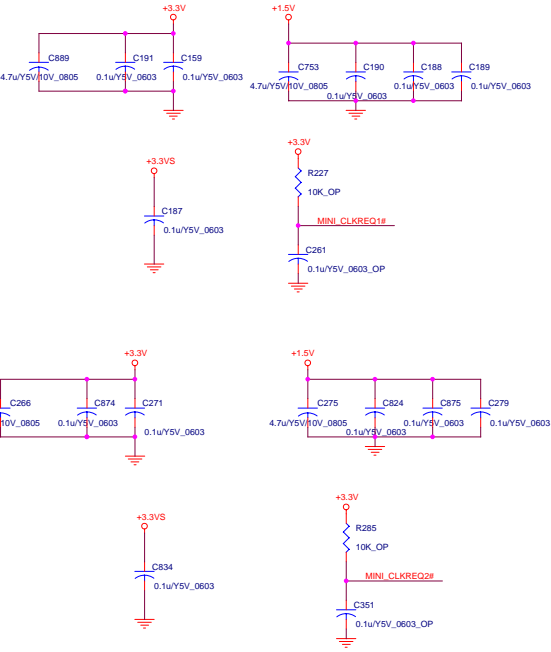
RAID CONN



MINI CARD CONN

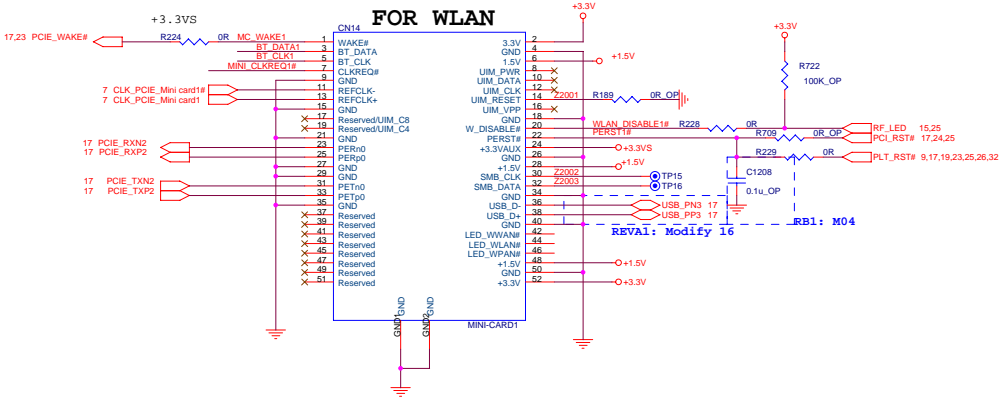
Intel PRO/Wireless 2100 LAN

PIN1	LED_WLAN_LINK	Hi(1.3V) Low(0V)	Solid ON LED OFF	Associated AP Not Associated with an AP Power OFF or RF Kill active
PIN2	LED_WLAN_ACT	Hi(1.3V) Low(0V)	Rapid Blinking Slow Blinking	Passing data traffic to AP Beacon traffic to AP Power OFF or not activity or RF Kill active
PIN3	HW_RadioXMIT_OFF#	Hi(1.3V) Low(0V)	Enable Disable	Radio transmitter is ON Radio transmitter turn off

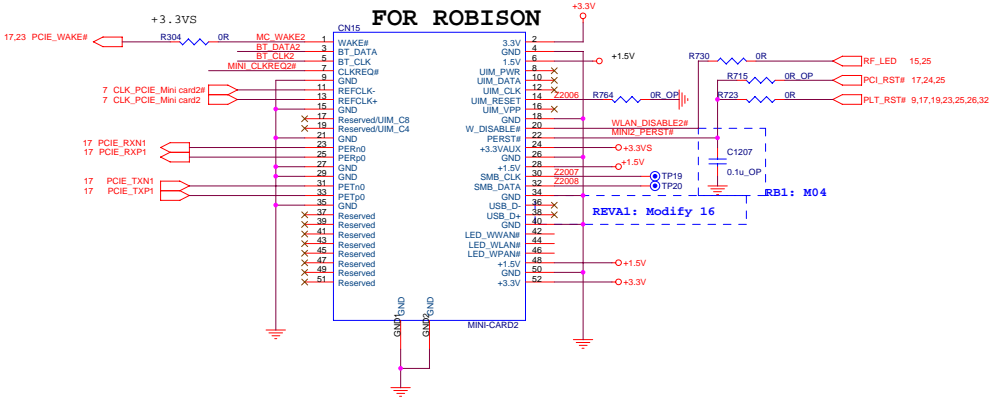


BT_DATA1 21
BT_CLK1 21

FOR WLAN

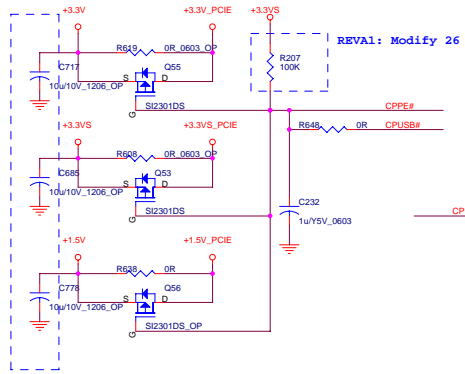


FOR ROBISON

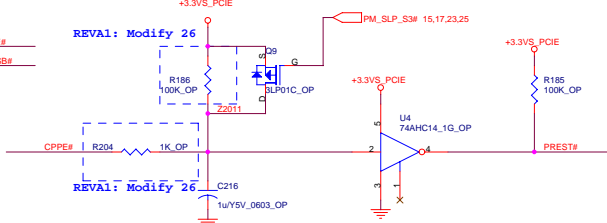


NEW CARD Socket

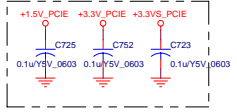
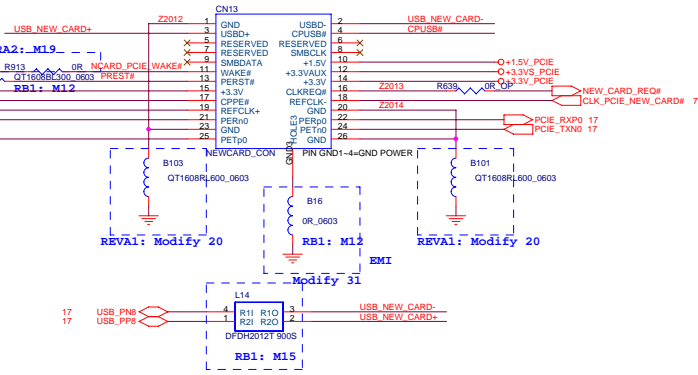
REVAL: Modify 26



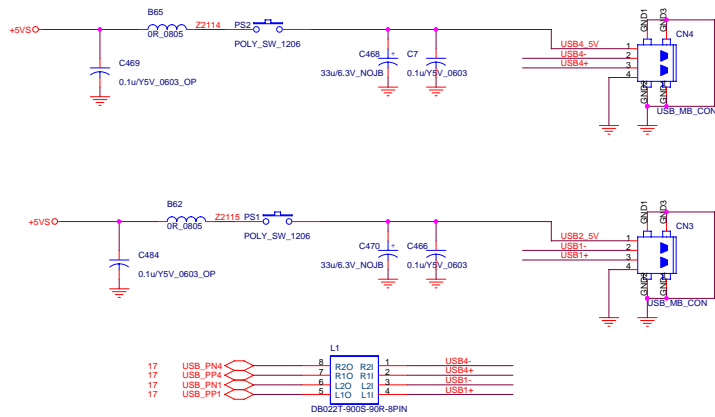
REVAL: Modify 26



REVAL: Modify 26

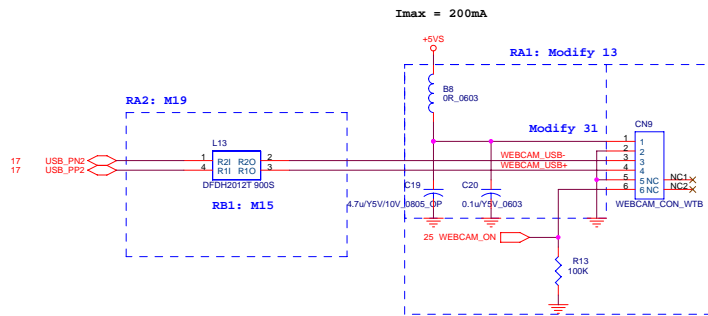


USB PORT CONN

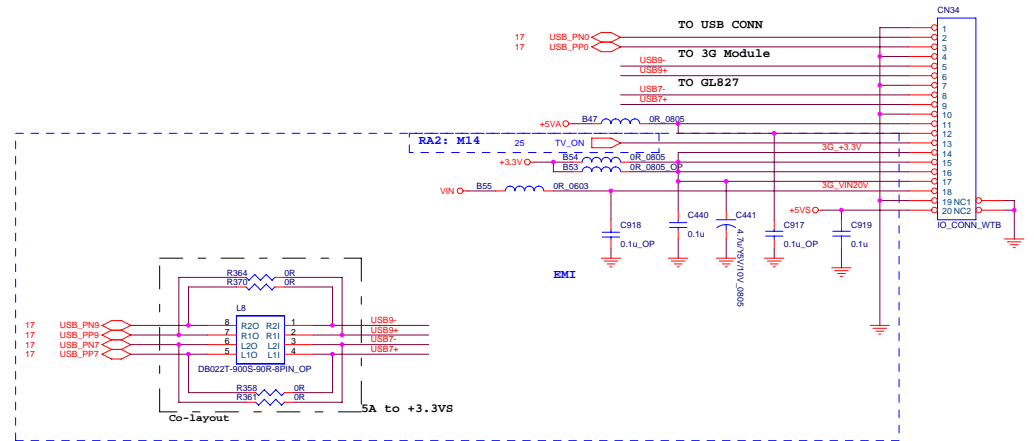


USB CONN change from 3 ports to 2 ports @ REVA2
One USB ports W/I charger remove to daughter board and add eSATA port@ REVA2

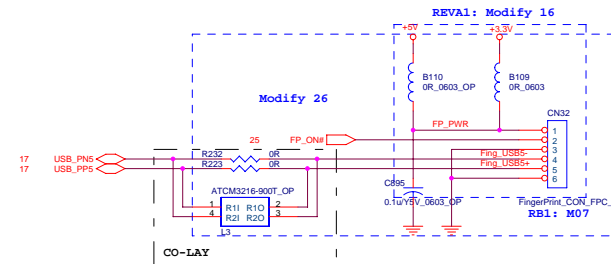
WEBCAM CONN



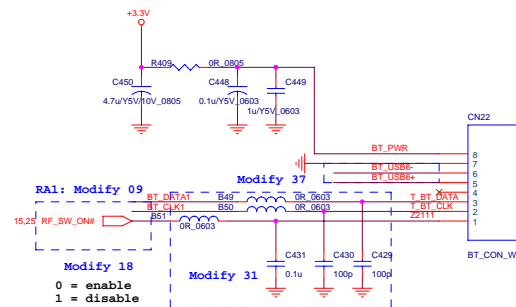
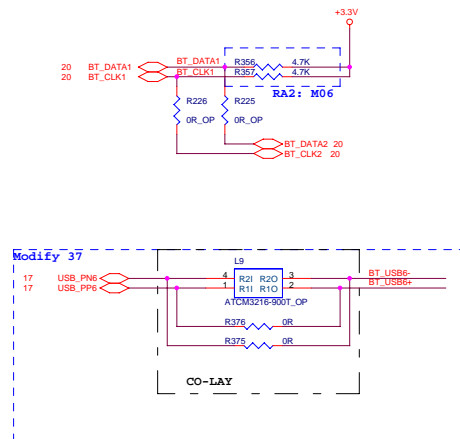
IO PORT CONN



Finger print CONN (P75 only)



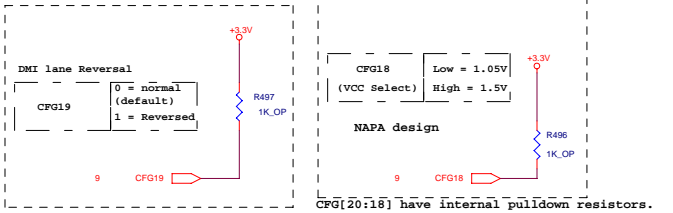
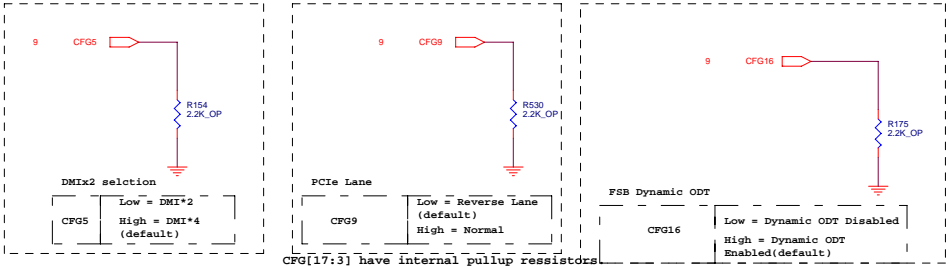
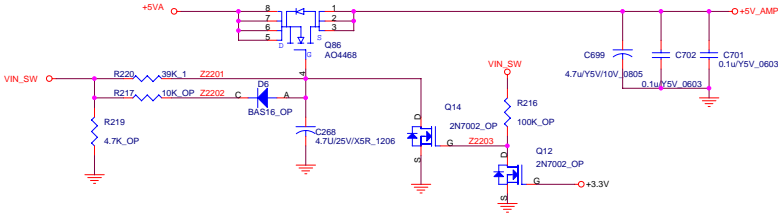
BLUETOOTH CONN



UNIWILL COMPUTER CORP.

File	P75/55IMx		
Size	3831	Document Number	Rev C
Date	Tuesday, March 13, 2007	Sheet	21 of 37

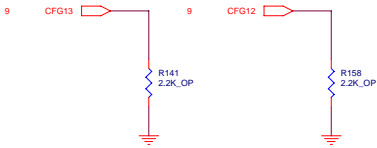
AMP VDD



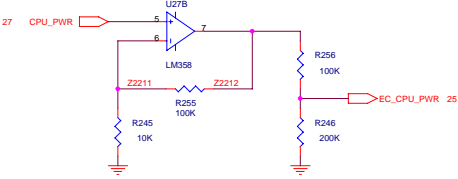
CFG20
(SDVO/PCIE Concurrent Operation)

0 = Only SDVO or PCIE x1 is operational (default)
1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

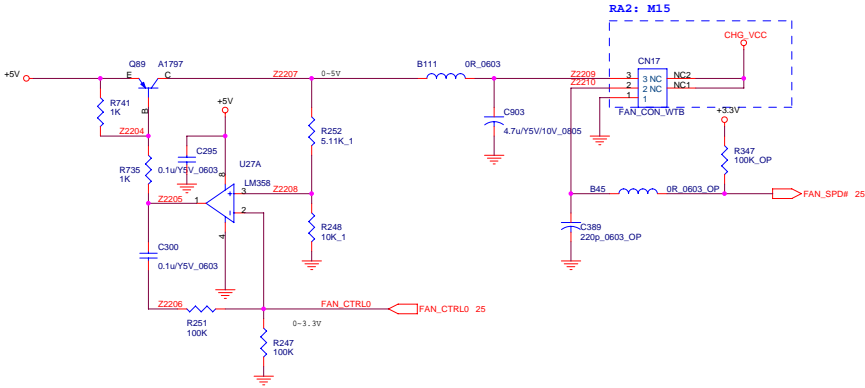
XOR / ALLZ / Clock Un-gating		
CFG12	CFG13	Configuration
0	0	Clock Gating Disabled
0	1	XOR Mode Enabled
1	0	All-Z Mode Enabled
1	1	Normal Operation (Default)



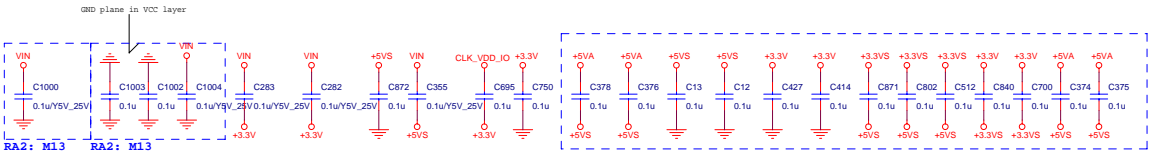
CPU POWER MONITOR



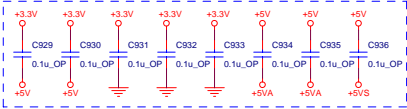
CPU FAN CONTROL

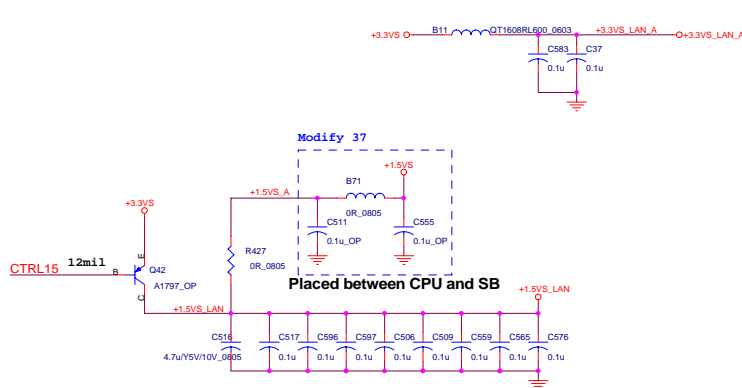


High speed current return path Capacitor



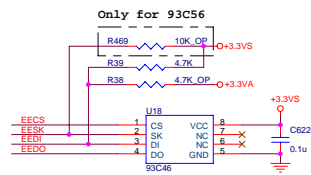
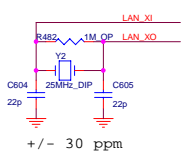
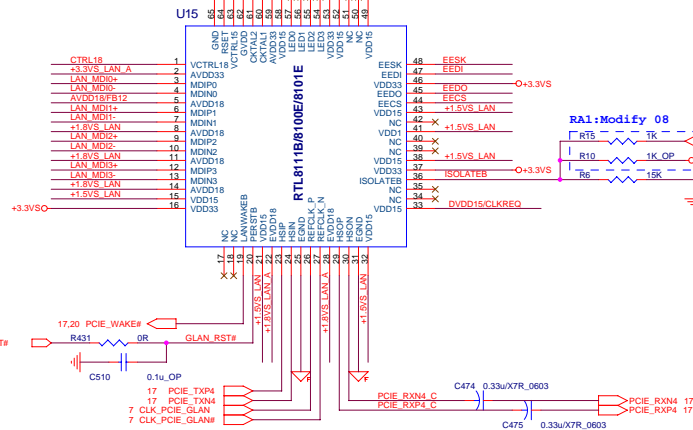
EMI Reserved





R65 is only used for RTL8111C application.
For RTL8111B/8101E remove R65.

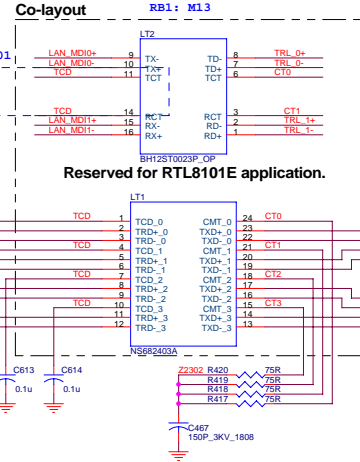
R474 value should be 2.49K (1%) for 8111B/8111C application
R474 should be 2.0K(1%) for 8101E application



Power domain chart

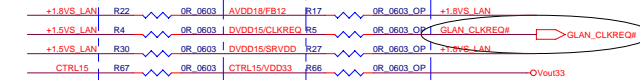
	RTL8111B/ RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

	Q44	Q43
RTL8111B	Need	Need
RTL8111C	N/A	N/A
RTL8101E	N/A	N/A



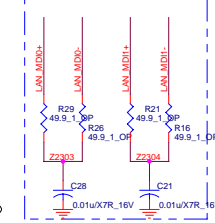
Remove R911 for 8111B and 8111C

For RTL8111B/8101E application.



Reserved for RTL8111C application.

Reserved for RTL8101E application.

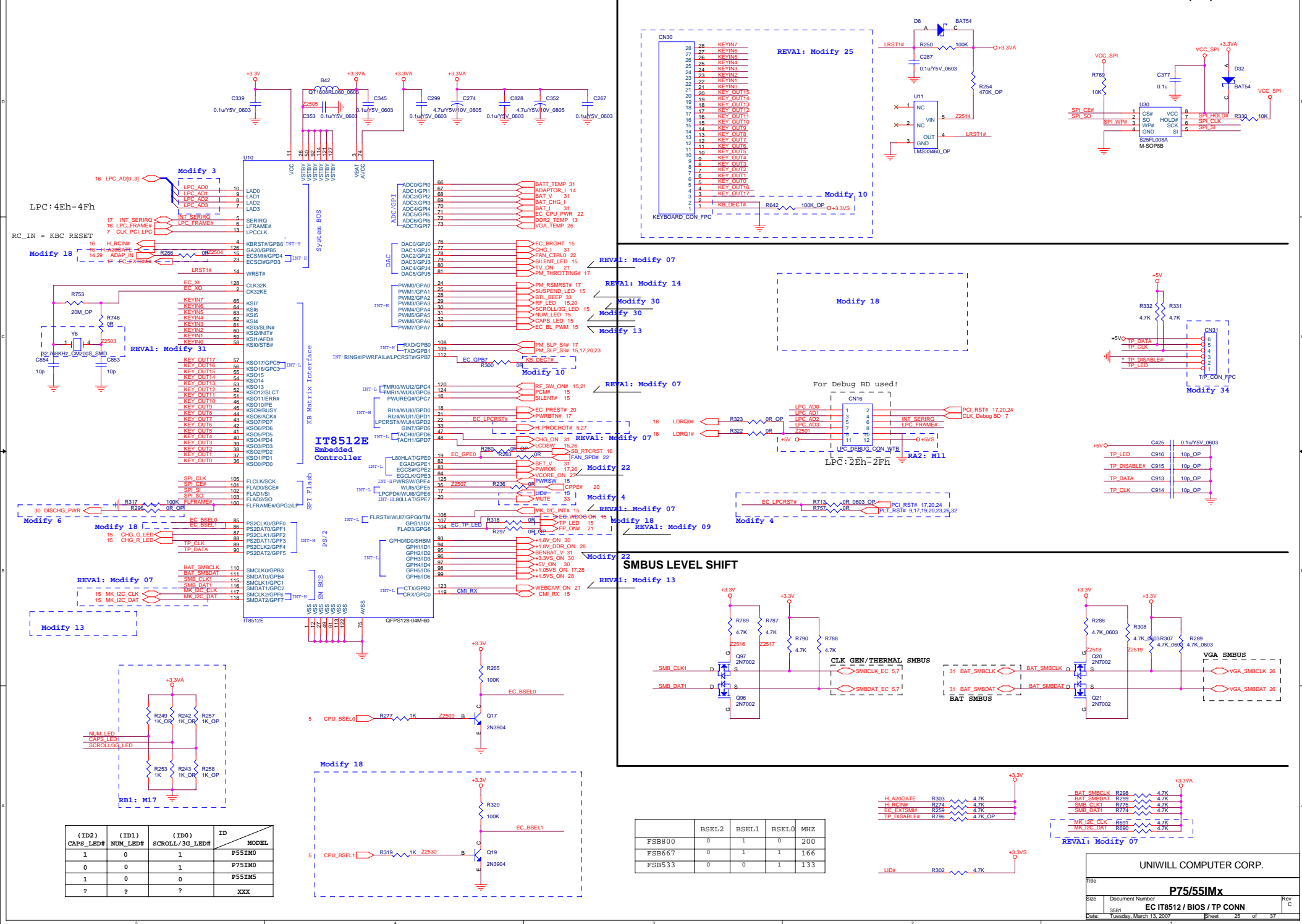


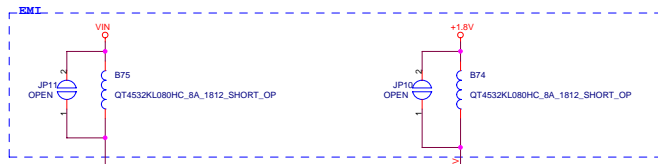
Reserved for RTL8101E application.



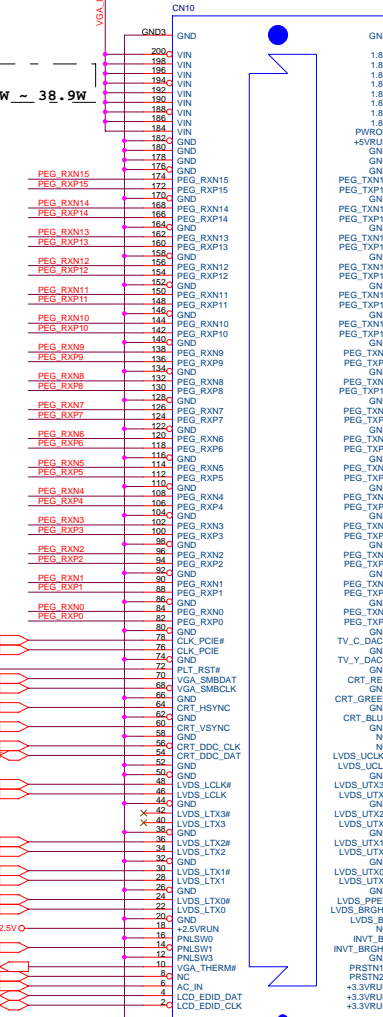
UNIWILL COMPUTER CORP.

Title		P75/55IMx	
Size	Document Number	GIGA LAN (Intel 82573L)	
Date	Version	Sheet	23 of 37





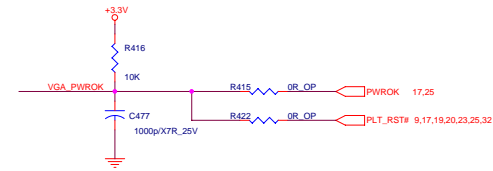
VIN:
7.5V to 22V / 4A 8.9W ~ 38.9W



1.8V+-5% / 3.5A_6.3W

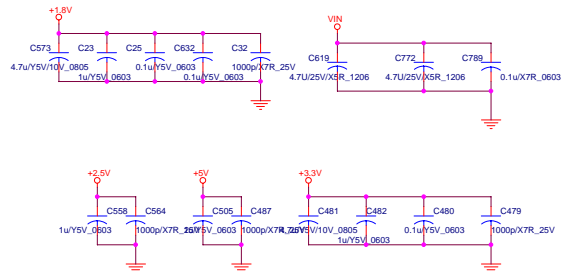
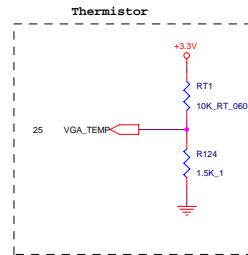
5V+-5% / 0.5A_2.5W

3.3V+-5% / 1.5A_4.95W

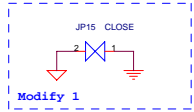


PEG_TXN15.0] PEG_TXN15.0] 9
PEG_TXP15.0] PEG_TXP15.0] 9

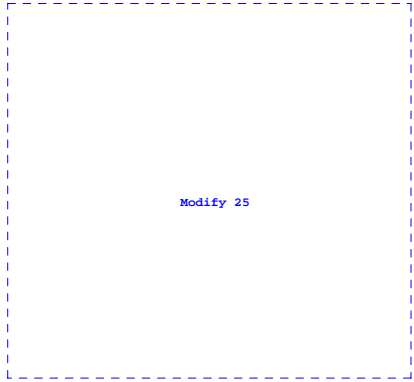
PEG_RXN15.0] PEG_RXN15.0] 9
PEG_RXP15.0] PEG_RXP15.0] 9

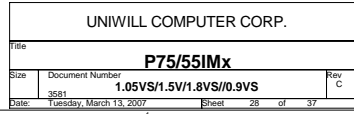


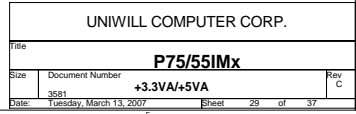
UNIWILL COMPUTER CORP.			
File	P75/55IMx		
Size	Document Number	VGA MXM CON	
Custom	369	Rev C	
Date:	Tuesday, March 13, 2007	Sheet	26 of 37

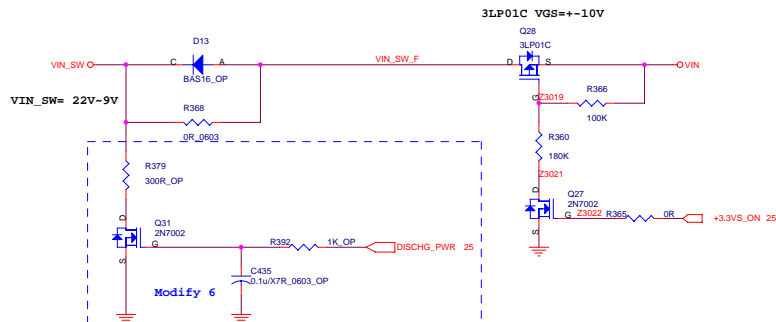
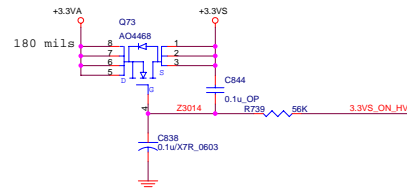
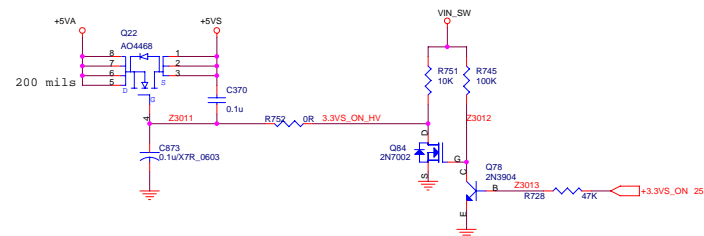
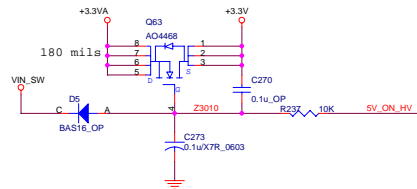
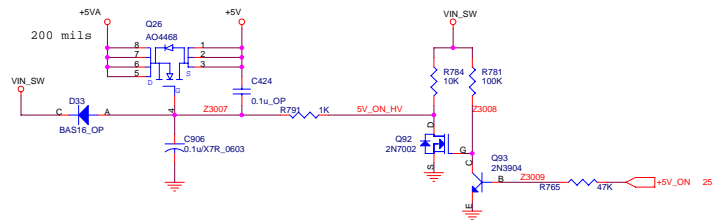
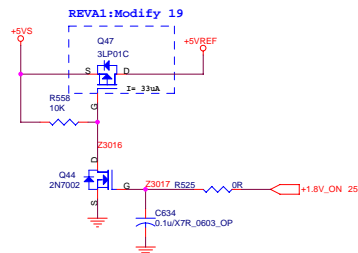
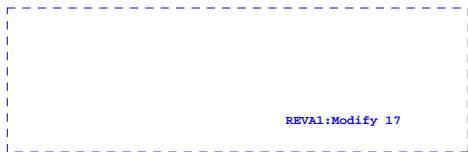
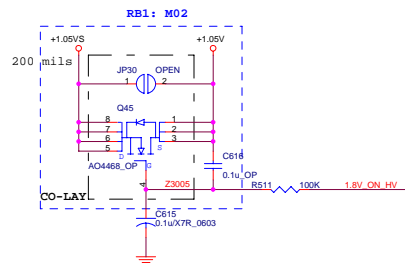
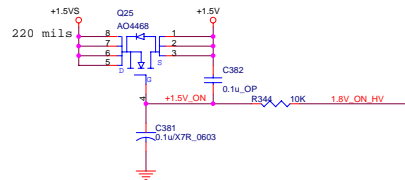
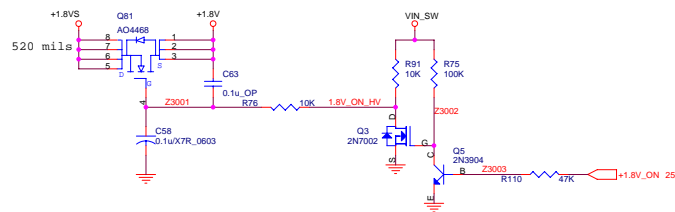


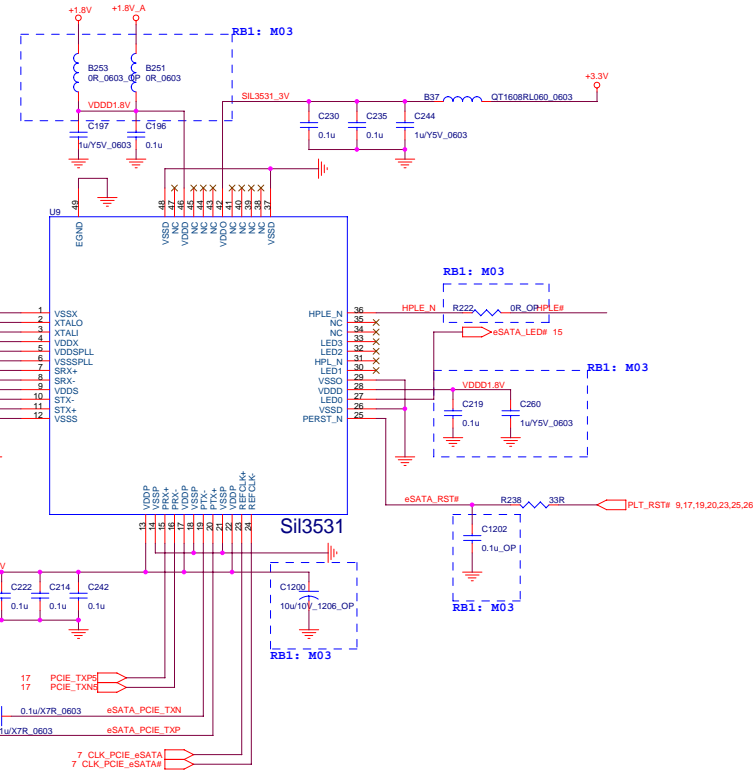
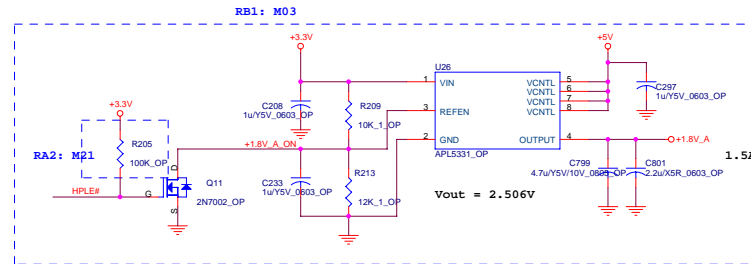
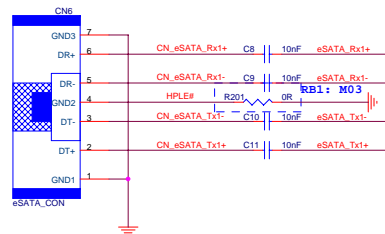
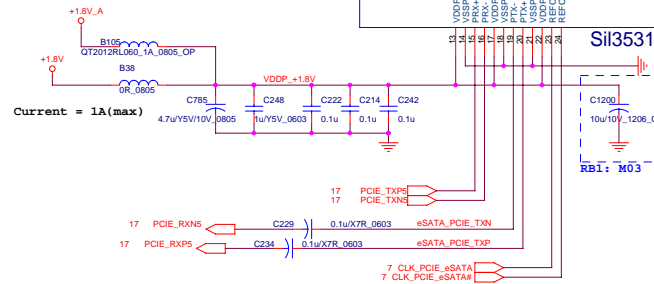
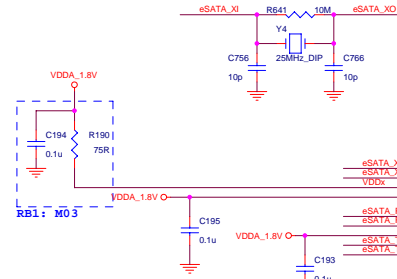
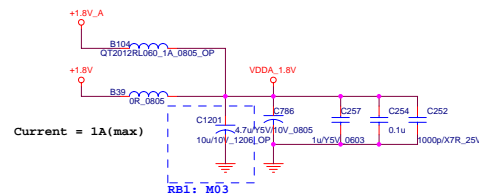
6	5	4	3	2	1	0	Vcore	Status
0	0	1	0	0	0	1	1.2875	(HFM)
0	0	1	1	0	0	0	1.2000	Boot Vout
0	0	1	1	1	0	0	1.1500	Mem0(HFM)
0	1	1	0	0	0	1	0.8375	Y&M(LFM)
0	1	1	1	0	1	0	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	0.0000	Shut down



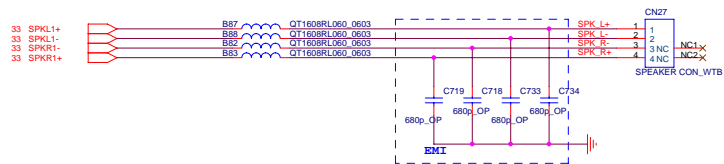




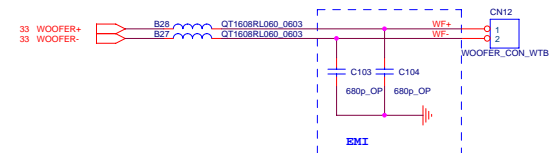




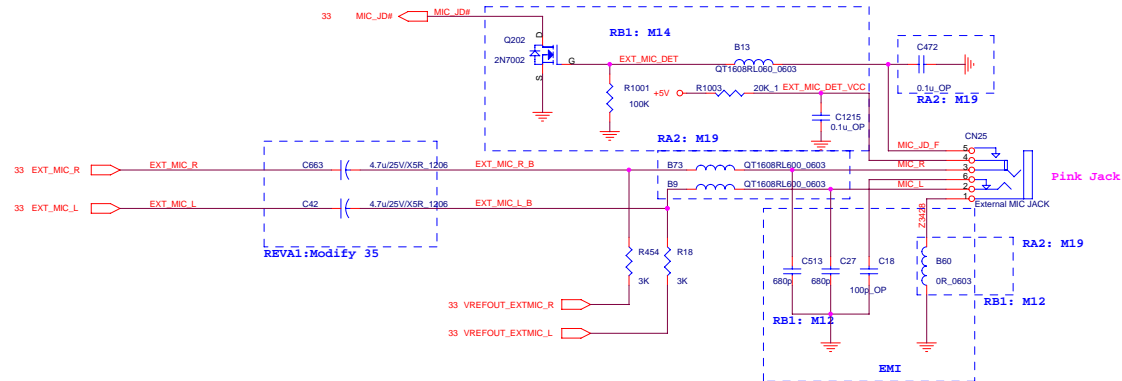
Internal SPK



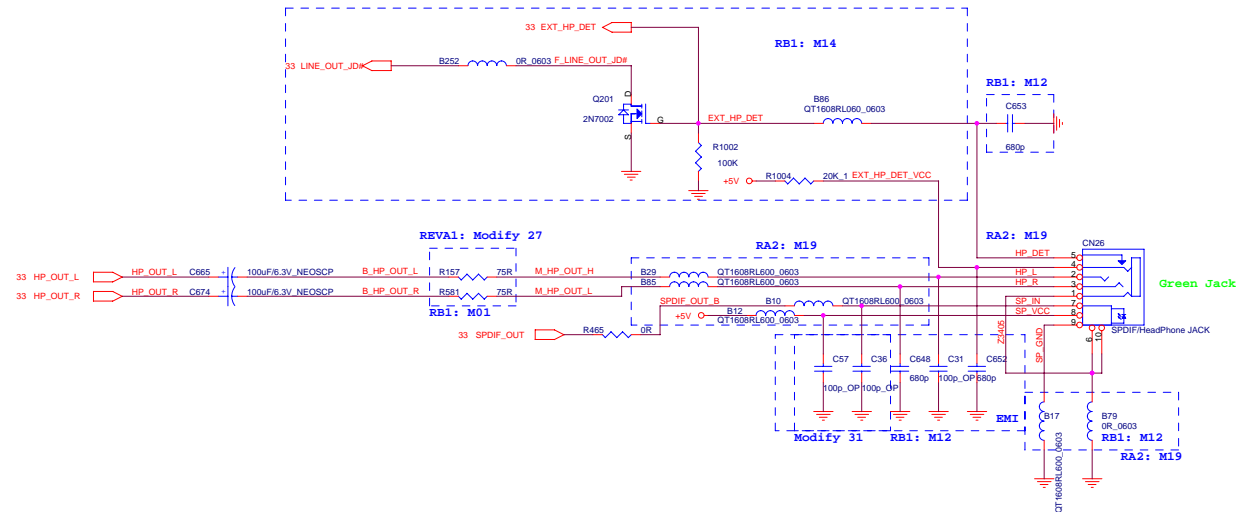
Woofer



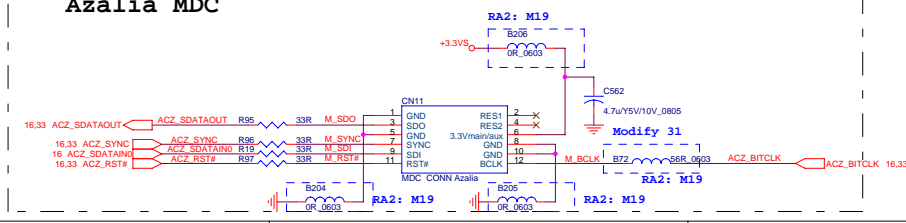
External Mic



SPDIF/HeadPhone



Azalia MDC



UNIWILL COMPUTER CORP.

Title		P75/55IMx	
Size	3631	Document Number	PHONE JACK & CONN & MDC
Date:	Tuesday, March 13, 2007	Sheet	34 of 37

RA change list:

Symbol	What change	Page	Why change	Note
Modify 1	Add Jump JP19 to conect AGND and GND	27	Presenting from other project mistake	
Modify 2	R8 from +CPU_CORE change to GND	6	Mistake net	
Modify 3	LPC AD0 ~ AD3 mistake	25	Mistake net	
Modify 4	PLT_RST# and MUTE swap	25	Follow older version and pin assingment	
Modify 5	+1.5V changed to +1.05V	9	Mistake net	
Modify 6	Add Q200, R900 and changed EC's MPWORK to DISCHG_PWR	25&30	VIN_SW discharge circuit	
Modify 7	Take out R669, C713 and mount R682 and changed MPWORK to PWROK	17	Follow Intel recommend	
Modify 8	Add R901,R900 and net: ICH_GPIO10, ICH_GPIO14	17	Follow Intel recommend (AMT didn't supported AMT)	
Modify 9	U32(1394) change IRQ form INT_PRIQC# to INT_PIRQE#	17&24	For blance IRQ routing	
Modify 10	Add R903 100K_OP, TP50, TP51, and change from QRT_STATE to KB_DETECT	17&25	For P75 K/B automatic detect.	
Modify 12	U8 form JMB363 change to JMB362 and other	17&32	cost down solution and form PCIE6 change to PCIE5 by SW required	
Modify 13	Add C1000(0.1u.0603) and C1005(4.7u.0805)	21	Reserved for power bypass and EMI	
Modify 14	Add RP20, RP21 0 ohm and take out L10&L11	23	Reserved for replace com-choke	
Modify 15	Add R910 and change R347,R351(24.9->29K), R137,R151(4.7K->0R), R167(49.9K->0R) and take out R131,R152 ,R568, R142	19&33	Adjust Audio gain	
Modify 16	Change R170 to pull high +3.3V and take off R554(0R)	07&17	Solving for C3 hand up	
Modify 17	Del R487/R492(OR_OP), JP1, R36 and swap net:M358+/- net ; CN11 change type	21	Delete reservedcircuit and swap wrong net ; CN11 by ME required	
Modify 18	Add R904(100K), R905(1K), Q201, net: BSEL1 tired to GPF1 and net:ADAP_IN from GPF1 to GPD4 ;	05&25	For support CPU of FSB 533	
Modify 19	C49&C50 from DIP change to SMD; Mount_Q6,Q52,Q8,Q53,Q12,R165/R176, R640,R189,R194,C709 ; take out R161,R179	05&25	For ME limit and POP nose / Head phone POP nose	
Modify 20	Add R911,R912(OR_0603)	29	Resistor reserved for fine tune	
Modify 21	Take out R618(10K)	17	Pull high wrong power plane	
Modify 22	Delete R837 and JP17; R412,R409,R416,R407,R831,R835,R834,R411, U47 and R832,R836,R840 Change R406(127K->20K_1), R410(127K->1.5K_1), R414(1M->0R_0603), R404(1M->1.6.5K),R830(1K->1.5K), C898(0.1u->1u_0603) C900(0.1u->0P), and add D50	31	For dumb bettery	
Modify 23	Add R914,R913(0R) , C1007(0.1u), C1008(4.7u), C1006(0.1u), CN37	20&21	Reserved for support P75 TV and 3G together	
Modify 24	Max8776 change to OZ811	35	Delete GXP power(965GM) and Add +1.05VS power	
Modify 25	Delete Q91, Q84, Q83, Q90, R774, R725, R726, C817, C324,C308, C294, C776, C826, C214, RT4	27	Delete reserced power circuit	
Modify 26	Add R916, R915(OR), R917,R918(OR_OP) and CN38	20	Reserved for P75 function of Figer print	
Modify 27	L14 from FRCL1394 change to ATCM3216 and Add L20	21	CN5 and CN11(USB) split, cause of ME change location	
Modify 28	Change U43 package from MOS-8 to PMOS-8 and U40 mount	28	For support to supply higher current (1.8V:10A ; 1.05V :2.1A max)	
Modify 29	R387 change from 5% to 1%	31	For improve accurate charger current	
Modify 30	CAPS_LED and SCROLL/3G net swap	25	EC required	
Modify 31	Deleted R95 and add B102 ; Deleted R14 and add B103 ; Deleted R10/R11 and add B101 / B104 ; C1000 Deleted R382,R383,R384 and add C1013,C1014,C1015 ,B105 ,B106, B107 , Deleted C895,C896, C899 ; deleted R838,R839, and addB108,B109,B112,B113	15&21 & 34&31 & 20	EMI required	
Modify 32	Add Q209, D53	33	For sus-woofer can't mute by codec issue	
Modify 33	Add L21 and delete JP15,B86	27	Co-layout reversed for improve Vocre effect	
Modify 34	CN35 change footprint from 0.5mm to 1.0mm pinch	25	ME required!	
Modify 35	Add B110 to +1.5V and take out B67	7	CLK_GEN power saving	
Modify 36	Add C1018,C1031,C1028,C1022,C1024,C1026,C1029,C1023,C1027, C1030,C1016,C1020,C1019,C1025,C1017,C1021,C1032	15	EMI required	
Modify 37	Add L22_OP and RP22 co-layot and change USB pair ; Add C1033,C1034(OP) and B111	21	EMI required (B111 for +1.5VS cross CLK_GEN)	

RA2 modify list:

Symbol	What change	Page	Why change	Note
RA2: M18	Add C1002/C1003 0.1u Add C1004 0.1u_25V	36	For PCIE6 pair current return path For USB0 pair current return path(remove trace to improve)	
RA2: M19	Add C1005/C1001 0.1u/YSV 25V Mount L13 DFM2012 300S DINTRECH ; take out R430/R429 OR Add B204/B205/B206 OR_0603 Take out C472/860/B797/C471/C488/C653 B25 from AMC1608Q600NT change to QT1608RL300HC2A R551 from OR change to 100K R80/R18 from OR OR_0805 change to QT2012RL120HC3A-LF_0805 B72/R540 from 33K change to 56K B17 from OR_0603 change to QT1608RL600_0603 B10/B12 from QT1608RL060 change to QT1608RL600_0603 Add R913 OR Add B207/B208 OR_0603 Add C1006-C1011 0.1uF_0603_OP B29/B85/B73/B9 change to OR_0603	14 21 33&34 20 13 13 33&34	Reserced for EMI required	EMI memo 2.0
RA2: M20	Add C1012/C1014 OR_0603 ; C1013/C1015 OR_0402	15	Reserced for RAID unstable issue	
RA2: M21	R205 mount 100K	32	eSATA CONN detect pull high	
RB: M01	LT2.3/LT6.6 change to tie to TCD	23		

RA1 change list:

Symbol	What change	Page	Why change	Note
RA1: Modify 01	Add D60 BAT54 between ODD and LED	15	Solving ODD detect fail within HDD issue(BIOS can't detect ODD master or slave)	
RA1: Modify 02	B42 change from QT1608RL060_0603 to QT2012RL030_3A_0805	19	Reserved for more power consumption ODD as HD-DVD	
RA1: Modify 03	Net changed SMBCLK and SMBDAT to ICH_SMBCLK and ICH_SMDATA	17	Net disconnect from SB to CLK GEN	
RA1: Modify 04	R449,R450,R451	9	Intel recommend	
RA1: Modify 05	U24.F20(LAN_TX1-) change to U24.E20	16	update library	
RA1: Modify 06	Net: CRB_SV_DET pull high from +3.3V to 3.3VS	17	Pull high power wrong	
RA1: Modify 07	Change CN26 to 20 pin and add net: MK_I2C_DAT/CLK/INT# to KBC and LED signal Change Net:Mail# to SB_RTCSRST to MK_I2C_INT# and SMP1_EN# to H_PROCHOT to MK_I2C_DAT Net: BROWSER# rename to PCN#	15 & 25	For multimedia bottom function used ; Reserved to P75 LED BD	
RA1: Modify 08	Take out R12(1K) and mount R17(1K)	23	Solving +3.3V leakage during power on and S3	
RA1: Modify 09	Net: BT_ON# change to FP_ON# and BT_ONchanged to RF_SW#	15/2125	KBC change GPIO to FP_ON# (Finger print ON)	
RA1: Modify 10	Max8744 pin31 tied to net change from VL to 8744REF	29	FAB recommend(voltage rating of FB pin is VLDO+0.3V only)	
RA1: Modify 11	Add net: RAID_CONF0-3 and CN36/CN41	17 & 19	Reserved for P75 H/W RAID configuration setting and CONN	
RA1: Modify 12	Mount R554	17	Implement STP_CPU(NB CLK set Free run)	
RA1: Modify 13	CN9 4P->6P, add net: WEBCAM_ON to EC, deleted +5V power	21 & 25	Implement WEBCAM ON/OFF function	
RA1: Modify 14	Net: Silent LED and BREP swap	25	BREP should be generated by EC's PWM	
RA1: Modify 15	Delete L21	27	Delete reserve function	
RA1: Modify 16	USB pair change USB3 to USB5 and CN38 4P->6P and add net:FP_ON#	20 & 21	Implement Finger print ON/OFF function	
RA1: Modify 17	U3/U5 VIN change from +1.8VS to +1.8V and deleted enable; Delete Q46, C598, R543,C596	28 & 30	+1.25VS LDO power change to +1.25V	
RA1: Modify 18	U40 Change from APL5331(2A) to APL5912(5A) and delete U10	28	APL5912 rating(5A) and dropout (200mV) better than APL5331	
RA1: Modify 19	Q47 change from SI2301 to 3LP01	30	Cost saving (VINSW current = 44uA)	
RA1: Modify 20	Add B203 OR_0805, B79/B80 QT1608RL600_0603 ; B66/B110 QT1608RL600HC-1A_0603	7/20/33	EMI requirement	
RA1: Modify 21	Add U50_OP and U4.7 change net to HDMI_SPDIF_ON#	33	U50 reserved for SPDIF buffer ; Could be controlled be codec	
RA1: Modify 22	Add net: MUTE	34	MUTE to controlled HP POP issue	
RA1: Modify 23	F2 0603->1206 ; R413 40mR->25mR ; R387 39K-> ??K ; Add R1003 100K / R925 100K->127K	31	F2 co-layout poly switch; combine with DC1	
RA1: Modify 24	Delete C148/C247 ; SRC11 change to RAID CLK	7	SPEC changed	
RA1: Modify 25	U32 from 24PIN to 28 PIN and deleted CN29	25	New K/B supported	
RA1: Modify 26	Add Cap reserved to power by pass ; change pull high power plane	20	Reserved for impovement power drop ; the circuit wrong	
RA1: Modify 27	Add R between HP R/L line	34	Reserved for HP amplitude requirement	
RA1: Modify 28	Take out R and C	33	Imporing background noise	
RA1: Modify 29	Add R between HP R/L line	33	Reduce amplitude to meet requirement	
RA1: Modify 30	Take out some component	33	Taking out reserved function	
RA1: Modify 31	Crystal change to SMD	16 & 25	Manufactory required	
RA1: Modify 32	Modify Charger circuit	14 & 31	Reference DC1 circuit and hope to improve yield	
RA1: Modify 33	Modify Cap value	07 & 24	Fine tune crystal precision	
RA1: Modify 34	R change from 100K to 31.6K	15	PWM inverter sink current higher	
RA1: Modify 35	CD tired to GND ; MUTE function ; LINE IN Cap	33 & 34	Vista not support analog ; ADI can't lost ; AP measure fail	

RA2 modify list:

Symbol	What change	Page	Why change	Note
RA2: M01	Mount R647/R692/R693/R694 4.7K; R673/R748/ 1K; R676/R679/R727 OR; R240 1K OP Deleted Q76_OP; Add R912 100K	14	For implement smart power function	
RA2: M02	Add R900 4.7K OP	29	Reserved for AC fast plug in/out fail issue	From DC1 recommend
RA2: M03	Add R904/R906 10K, R902/R903//R905/R907/R908R909 10K_OP Mount R339 10K	15	Solving LED flash when main power insert first For RAID LED pull high	
RA2: M04	Mounting D29 and deleted JP12 ; TL594.9 tried to GND	14 & 31	D29_OP made leakage ; mistake net.	
RA2: M05	C50 remove co-lse to IC , R106 pull high from 3.3V change to APA_5V U21 package from LQFP48/QFN change to QFN48	33 & 34	Solving POP noise Manufactory requisition	
RA2: M06	Mounting R356/R357 4.7K	21	Implement WLAN and Buletooth coexistence function	
RA2: M07	R9 from 24_9R_1 change to 56R R57 from OR change to OR_OP and add R910 OR DM1_ZCOMP pull high power from +1.5V change to VCCA3GP R515/R564/R565/R930/R938/R550/R1353/R398/R534 from OR change to 10K R672 changed form 1K_1 to 392R_1	05 17 09	Intel recommend	
RA2: M08	Mounting C320 820uF/2.5V and delete C319 220uF/6.3V C388 from 220uF/6.3V_SMT change 820uF/2.5V_DIP R785 from 43.2K_1 change to 51.1K_1	28	Manufactory requisition (don't co-lay) and cost saving Cost saving Increasing +1.05VS to +1.1VS, prevent voltage drop on the end	
RA2: M09	Add D50-D51 UD23V3/0.2W_OP	15	Reserved for FPC cable shift and made EOS issue	
RA2: M10	Add R911 OR_0603_OP	23	Reserved for RTL8101E	
RA2: M11	CN16.11 power from +5VS cahnge to +5V and add pin12 to +5VS	25	LPC is used to normal 5V power plane	
RA2: M12	R731 mount OR	27	Correcting schematic (VRHOT# is OD INPUT)	
RA2: M13	C153/C145 from 3900pF_0603 change to 0402 R629 from 24_9R_1 change to 18R_1 Add C1000 0.1uF/25V R807 mount OR	16 22 19	For share the same component on BOM Increasing SATA driving stream to meet eye pattern measure For SATA current return path For SATA spec requirement	
RA2: M14	EC GP44 from SMP1_EN#(SB_RTCSRST#) change to TV_ON EC_GPB6 change to PAN_SPDW(SB_RTCSRST) SMP1_EN# from EC_GP44 change to ICH_GPIO2	21 & 25 19 & 25	Add TV ON function	
RA2: M15	CN17 from Vertial change to right angle (88267-0300)	22	Reserved for support VGA type III	
RA2: M16	C61 100uF_DIP change 4.7uF/6.3V_0805	33	Solving POP noise	
RA2: M17	Add B200-B203 OR_0603_OP	13	Reseved for EMI	

*Note: After item of RA2: M18, please seem appendix A

Uniwill International Corp.			
File	Appendix A. Ver.AtoA1 History		
Size	Document Number	P75/55IMx	Rev C
35g	Date	Tuesday, March 13, 2007	Sheet 38 of 37

*** Rev.B to B1 whcih was changed Codec from ADI1986A to ALC883 ***

RB1 modify list:

Symbol	What change	Page	Why change	Note
RB1: M01	Add R553 20K_1 ; HP R/L SWAP ; R157/R581 0R->75R Net: SR_OUT_R/L changed channel from sidesurround to surround	33 & 34	The codec's sense resistor miss ; tried wrong net ; AP measure Following up L50II0 pin definition	
RB1: M02	Add JF30 co-lay with Q45 and take out Q45	28 & 30	Power on sequence to simplify and improved MOS Rds(ON) lose and cost saving.	EC change "+1.05VS_ON" sequence to follow "+1.8V_ON"
RB1: M03	Mount U26 APL5331, C208/C297/C233 1uF_0603, R209 100K_1, R213 120K_1, C799 4.7uF_0805 and R222 0R/ R205 100K take out and mount R201 0R Add C1200/C1201 10uF_1206_OP and C1202 0.1uF_OP and B251 0R_0603 and C194 cahnge net form VDDX to VDDA_1.8V	32	Solving PCIe unstable and auto reset issue Resversed for improve power ripple and platform reset nose and Vendor recommend improved for IC's power	
RB1: M04	Add C1203/C1204 0.1uF, C1205/C1206/C1207/C1208 0.1uF_OP			
RB1: M05	Swap net: PWR5W, LID#, FAN_SPD# and update project ID table	25	For support wake up function and sort PCBA REV.B or REV.C	
RB1: M06	R902 mount 10K and add C1209 0.1uF_OP	15	Solving suspend LED flash when first plug-in power and resversed ESD issue	
RB1: M07	Take out CN32	21	FP CONN take out	
RB1: M08	C827 package change form 0805 to 0603 R734 change form 71.5K to 36.1K_1; R744 change form 4.75K to 6.89K_1	27	0.22u/X7R 25V 603 package is public C827 package change form 0805 to 0603	
RB1: M09	Add C1201 0.1uF_0603_OP	14	Resversed for EMI	
RB1: M10	C926 change form 0.1uF_OP to 1uF_0603	31	Improved for BAT_I signal	
RB1: M11	Add C1211-C1214	22	EMI required	
RB1: M12	C325, C301, C324, C302, C331, C305 mount 0.1 u C648, C653, C652, C513,C27 mount 680p; B60, B79 mount 0R B16 Q1608RL600_0603 -> 0R_0603, R627 0R->QT1608BL300_0603 Add C1216/C1217 0.1uF	15 34 20 15	EMI required (EMI memo 2.2) EMI required (EMI memo 3.3)	
RB1: M13	RT2 roatae 180 degree(library modify)	23	Improvement 10/100 LAN signal	
RB1: M14	Add Q200-Q202 2N7002, R1000-R1002 100K, R1003/R1004 20K_1, C1215 0.1uF_OP, B252 0R_0603 and add net: CODEC_OP1D0	33 & 34	Realtek recommend circuit	
RB1: M15	L13/L14 change layout footprint and delete R429/R430 0R_OP	20 & 21	Improvement SMT	
RB1: M16	R92/R93 0R-> 10K , Add R1005/R1006 1K	33	Improvement MIC quality	
RB1: M17	R258 1K->0P, R242 1K->0P, R249 1K->0P, R253 mount 1K	25	For support wake up function and sort PCBA REV.B or REV.C	